Mohamed S. Abdelfattah

Born: August 8, 1988
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Education

2011-2016 PhD in Computer Engineering, **University of Toronto**, Canada
- GPA: 4.0, Advisor: Prof. Vaughn Betz
- Thesis: Architecture and CAD for Embedded Networks-on-Chip on FPGAs
- Vanier Canada Graduate Scholarship (Canada's highest doctoral award)

2009-2011 MSc in Information Technology, **University of Stuttgart**, Germany
- GPA: 4.0, Advisor: Prof. Hans-Joachim Wunderlich
- Thesis: Evaluation of Advanced Techniques for Structural FPGA Self-Test
- DAAD Scholarship

2005-2009 BSc in Electronics Engineering, **German University of Cairo**, Egypt
- GPA: 4.0, Advisor: Prof. Manfred Berroth
- Thesis: Design of an RF Transmitter for RFID Tags with Ultra-thin Silicon Substrates
- Gerhard Shröder Scholarship

Research & Work Experience

2019-Present Principal Scientist, **Samsung AI Center**, Cambridge, UK
I am leading a 5-person research team investigating the discovery, implementation and optimization of deep learning for constrained hardware using automated machine learning (AutoML). In one research stream, we used AutoML to find the best compression scheme for the speech model used for the Samsung Bixby virtual assistant. In another research stream, we are investigating the codesign of deep neural networks and their dedicated hardware accelerators using a unified AutoML formulation. Our most recent work tailors neural networks for different hardware targets both by modeling the hardware characteristics accurately and by improving neural architecture search efficiency to make device-specific AutoML possible.

2015-2018 Member of Technical Staff, **Intel**, Toronto, Canada
I worked on the development of Intel's FPGA machine learning accelerator (FPGA plugin for Intel OpenVINO Deep Learning Toolkit). I worked on many of the key hardware features that enable the high-performance implementation of deep convolutional neural networks. Additionally, I led the development of hardware and software to implement recurrent neural networks, with a focus on speech applications. Part of the work included the implementation of advanced compiler optimization passes for Intel's FPGA C-to-Verilog llvm compiler. Finally, I led a 4-person customer-focused team to integrate our accelerator within a commercial camera system.

Winter 2014 Research Intern, **Altera**, Toronto, Canada
I designed high-performance hardware for streaming Gzip compression on an FPGA. Additionally, I visited customers to present my Gzip compression hardware, which translated into design wins.

2011-2015 Research Assistant, **University of Toronto**, Toronto, Canada
I researched the addition of embedded networks-on-chip to modern FPGAs to facilitate system-level communication and to enable the deployment of complex applications to FPGAs. My research included architecture exploration, application case studies and computer-aided design. My work received three best paper awards and one nomination at international conferences. Additionally, my ideas had commercial impact when Xilinx and Achronix adopted networks-on-chip in their FPGAs.

Winter 2011 Research Intern, **Philips Healthcare**, Böblingen, Germany
I joined the IntelliVue patient monitor hardware team as they were transitioning from a custom chip to an FPGA for signal processing. I designed hardware that interfaces with other chips to analyze patient vitals such as heart-beat and blood pressure. Additionally, I created software using LabVIEW that automates part of the quality-testing of Philips medical devices.

2009-2011 Research Assistant, **University of Stuttgart**, Stuttgart, Germany
I researched the automated testing of FPGAs for partial reconfiguration. My research focused on exposing structural faults through a series of FPGA self-tests that target both logic and interconnect failures. If a fault is found, an FPGA circuit would then be relocated to another portion of the FPGA.

Summer 2008 Research Intern, **Mentor Graphics**, Cairo, Egypt
I led two teammates in the development of a program that translates various hardware descriptions of register files into a unified representation (based on the IPXACT standard). I rejoined the team in the following year to finalize the program, and it is now part of Mentor Graphics commercial toolchain.

Grants, Honours & Awards

Best Paper Awards

2016 (Runner-up) Michel Servit Award at FPL 2016 Conference
2015 FPL 2013 paper selected as one of the most significant papers in the first 25 years of the conference
2015 Best Paper award at FPGA 2015 Conference
2013 Stamatis Vassiliadis Best Paper Award at FPL 2013 Conference

Scholarships

2013-2016 Vanier Canada Graduate Scholarship (Canada's highest doctoral award)
2014 (Runner-up) Adel Sedra Distinguished Graduate Award
2012, 2013 Right Track CAD Graduate Scholarship (twice)
2011 Connaught Doctoral Scholarship Award
2009 DAAD Master's Scholarship Award
2007 GUC Gerhard Shröder Scholarship Award

Teaching *(University of Toronto)*

2016 TATP (University-wide) Teaching Award
2016 Faculty of Applied Science Teaching Award
2015 Department of Electrical & Computer Engineering Teaching Award

Publications

Conference Proceedings

Nov. 2021 **Temporal Kernel Estimation for Blind Video Super-Resolution**
Lichuan Chang, Royson Lee, Hongkai Wen, Mohamed S. Abdelfattah, Nicholas D. Lane
Computer Vision and Pattern Recognition (CVPR) [Submitted]

May 2021 **Zero-Cost Proxies for Lightweight NAS**
Mohamed S. Abdelfattah, Abhinav Mehrotra, Łukasz Dudziak, Nicholas D. Lane
International Conference on Learning Representations (ICLR) [Accepted]

May 2021 **NAS-Bench-ASR: Reproducible Neural Architecture Search for Speech Recognition**
Abhinav Mehrotra, Alberto Gil C. P. Ramos, Sourav Bhattacharya, Łukasz Dudziak, Ravichander Vipperla, Thomas Chau, Mohamed S. Abdelfattah, Samin Ishtiaq, Nicholas D. Lane
International Conference on Learning Representations (ICLR) [Accepted]

Dec. 2020 **BRP-NAS: Prediction-based NAS using GCNs**
Łukasz Dudziak, Thomas Chau Mohamed S. Abdelfattah, Royson Lee, Hyeji Kim, Nicholas D. Lane
Neural Information Processing Systems (NeurIPS)

Oct. 2020 **Iterative Compression of End-to-End ASR Model Using Reinforcement learning**
Abhinav Mehrotra, Łukasz Dudziak, Jinsu Yeo, Younyoon Lee, Ravichander Vipperla, Mohamed S. Abdelfattah, Sangjeong Lee, Daehyun Kim, Nicholas D. Lane
Conference of the International Speech Communication Association (INTERSPEECH)

Aug. 2020 **Journey Towards Tiny Perceptual Super-Resolution**
Royson Lee, Łukasz Dudziak, Mohamed S. Abdelfattah, Hyeji Kim, Stylianos Veneris, Hongkai Wen, Nicholas D. Lane
European Conference on Computer Vision (ECCV)

June 2020 **Best of Both Worlds: AutoML Codesign of a CNN and its Hardware Accelerator**
Mohamed S. Abdelfattah, Łukasz Dudziak, Thomas Chau, Royson Lee, Hyeji Kim, Nicholas D. Lane. *Design Automation Conference (DAC)*

Sep. 2019 **ShrinkML: End-to-End ASR Model Compression Using Reinforcement Learning**
Łukasz Dudziak*, Mohamed S. Abdelfattah*, Ravichander Vipperla, Stefanos Laskaridis, Nicholas D. Lane. *Conference of the International Speech Communication Association (INTERSPEECH)*

Sep. 2018 **DLA: Compiler and FPGA Overlay for Neural Network Inference Acceleration**
Mohamed S. Abdelfattah, David Han, Andrew Bitar, Roberto DiCecco, Shane O'Connell, Nitika Shanker, Joseph Chu, Ian Prins, Joshua Fender, Andrew C. Ling and Gordon R. Chiu
International Conference on Field-Programmable Logic and Applications (FPL)

Jun. 2018 **Harnessing Numerical Flexibility for Deep Learning on FPGAs**
Andrew C. Ling, Mohamed S. Abdelfattah, Shane O'Connell, Andrew Bitar, David Han, Roberto Dicecco, Suchit Subhaschandra, Chris N Johnson, Dmitry Denisenko, Josh Fender, Gordon R. Chiu
International Symposium on Highly-Efficient Accelerators and Reconfigurable Technologies (HEART)

Mar. 2018 **Flexibility: FPGAs and CAD in Deep Learning Acceleration**
Gordon R. Chiu, Andrew C. Ling, Davor Capalija, Andrew Bitar, Mohamed S. Abdelfattah
International Symposium on Physical Design (ISPD)

Sep. 2016 **LYNX: CAD for FPGA-based networks-on-chip**
Mohamed S. Abdelfattah, Vaughn Betz

International Conference on Field-Programmable Logic and Applications (FPL)

Dec. 2015 **Bringing programmability to the data plane: Packet processing with a NoC-enhanced FPGA**
Andrew Bitar, Mohamed S. Abdelfattah, Vaughn Betz
International Conference on Field-Programmable Technology (FPT)

Sep. 2015 **Design and simulation tools for Embedded NOCs on FPGAs**
Mohamed S. Abdelfattah, Andrew Bitar, Ange Yaghi, Vaughn Betz
International Conference on Field-Programmable Logic and Applications (FPL)

Feb. 2015 **Take the highway: Design for embedded NoCs on FPGAs**
Mohamed S. Abdelfattah, Andrew Bitar, Vaughn Betz
International Symposium on Field-Programmable Gate Arrays (FPGA)

May 2014 **Gzip on a chip: High performance lossless data compression on fpgas using opencl**
Mohamed S. Abdelfattah, Andrei Hagiescu, Desh Singh
International Workshop on OpenCL (IWOCL)

May 2013 **Augmenting FPGAs with Embedded Networks on Chip**
Mohamed S. Abdelfattah, Vaughn Betz
Workshop on the Intersection of Computer Architecture and Reconfigurable Logic (CARL)

Sep. 2013 **The Power of Communication: Energy-Efficient NoCs for FPGAs**
Mohamed S. Abdelfattah, Vaughn Betz
International Conference on Field-Programmable Logic and Applications (FPL)

Dec. 2012 **Design tradeoffs for hard and soft FPGA-based Networks-on-Chip**
Mohamed S. Abdelfattah, Vaughn Betz
International Conference on Field-Programmable Technology (FPT)

Jun. 2012 **Transparent Structural Online Test for Reconfigurable Systems**
Mohamed S. Abdelfattah, Lars Bauer, Claus Braun, Michael E Imhof, Michael A Kochte, Hongyan Zhang, Jörg Henkel, Hans-Joachim Wunderlich
International Symposium on On-Line Testing and Robust System Design (IOLTS)

Mar. 2011 **2.2 GHz LC VCO for RFID on a 0.5-μm digital gate-array for ultra-thin silicon substrates**
Mohamed S. Abdelfattah, Damir Ferenci, Markus Grözing, Manfred Berroth, Cor Scherjon, Joachim Burghartz. *German Microwave Conference (GeMiC)*

Aug. 2009 **Design of a RF Transmitter for RFID Tags in a New Tech. with Ultra Thin Silicon Substrates**
Mohamed S. Abdelfattah, Damir Ferenci, Markus Grözing, Manfred Berroth, Cor Scherjon, Joachim N Burghartz. *Workshop on Circuit Design and Digital Signal Processing (ProRISC)*

Journal Articles

Oct. 2016 **Design and applications for embedded networks-on-chip on FPGAs**
Mohamed S. Abdelfattah, Andrew Bitar, Vaughn Betz
IEEE Transactions on Computers (TCOMP)

Feb. 2015 **Power analysis of embedded NoCs on FPGAs and comparison with custom buses**
Mohamed S. Abdelfattah, Vaughn Betz
IEEE Transactions on Very Large-Scale Integration Systems (TVLSI)

Aug. 2014 **Networks-on-Chip for FPGAs: Hard, Soft or Mixed?**
Mohamed S. Abdelfattah, Vaughn Betz
ACM Transactions on Reconfigurable Technology and Systems (TRETS)

Feb. 2014 **The Case for Embedded Networks-on-Chip on FPGAs**
Mohamed S. Abdelfattah, Vaughn Betz
IEEE Micro Magazine

Book Chapters

Jan. 2015 **Embedded Networks-on-Chip for FPGAs**
Mohamed S. Abdelfattah, Vaughn Betz
Reconfigurable Logic: Architecture, Tools and Applications

Patents

Sep. 2020 **Method and Apparatus for Neural Architecture Search**
Mohamed S. Abdelfattah, Łukasz Dudziak, Abhinav Mehrotra
Application Number: UK2015231.0

Sep. 2020 **Method and Apparatus for Analysing Neural Network Performance**
Thomas Chau, Łukasz Dudziak, Mohamed S. Abdelfattah, Royson Lee, Nicholas D. Lane
Application Number: UK20199106.4

Sep. 2019 **Method for Designing Accelerator Hardware**
Mohamed S. Abdelfattah, Łukasz Dudziak, Thomas Chau, Royson Lee, Hyeji Kim, Sourav Battacharaya
Application Number: UK1913353.7

Apr. 2015 **Field Programmable Gate-Array with Embedded Network-on-Chip Hardware and Design Flow**
Mohamed S. Abdelfattah, Vaughn Betz
Application Number: US14060253

Teaching & Mentorship

Teaching

2014-2016 **ECE297 Communication and Design**: I was head teaching assistant, responsible for coordinating a team of 20 teaching assistants, leading tutorials with 100 students and mentoring students in the lab. I also worked on the course's redesign and wrote many of the assignments and code infrastructure. The redesign was very large in scope, transforming the course to a project in which students created a Google maps clone from scratch with graphics and algorithms on real world data. The overall course quality rating improved from 2.7/5 in the previous year to 4.3/5 after our redesign. My personal feedback score was a perfect 7/7 for both years – the only TA to get that mark.

2012-2015 **ECE241 Digital Logic Design and ECE243 Computer Organization**: Teaching assistant responsible for running labs, mentoring student groups in programming projects and grading assignments and examinations. My student evaluation scores were consistently above 6.5/7.

Student Supervision

2019-Present Co-supervising Master's student Alexander Eugen Irimiea with Prof. Nicholas Lane at the University of Oxford. He is researching the deployment of machine learning applications on low-power devices.

2017-2018 Supervised six interns during my time at Intel: Aidan Malone, Xinyu Liu, Prokhar Bhowal, Sherif Fawzy, Christopher Chu and Eugene Sha.

2015-2016 Supervised three students throughout their summer placement in our lab during my PhD: Ange Yaghi, Harshita Huria and Aya Elsayed.

Academic Service

2017-2018 Grant research program committee (Intel Representative)
NSERC Computing Hardware for Emerging Intelligent Sensing Applications (COHESA) Network.

Technical Program Committees

2019-present International Symposium on Field-Programmable Gate-Arrays (FPGA)
2017-present International Conference on Field Programmable Logic and Applications (FPL)
2018-present Artificial Intelligence Circuits and Systems (AICAS)
2017 International Conference on Field-Programmable Technology (FPT)
2016 International Workshop on Network on Chip Architectures (NocArc)

Journal Reviews

Since 2018 IEEE Transactions on Computer-Aided Design (TCAD)
Since 2016 IEEE Transactions on Computers (TCOMP)
Since 2015 IEEE Transactions on Very Large Scale Integrated Circuits (TVLSI)
Since 2015 ACM Transactions on Reconfigurable Technology and Systems (TRETS)

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